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Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/767,555 | CHOI ET AL. | |
| | Examiner | Art Unit | |
| | Michael Krofcheck | 2186 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *30 June 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-34 and 36-79* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-34 and 36-79* is/are rejected.

7)☒ Claim(s) *53, 57, 72, 76, 78* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 January 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

1. This office action is in response to the amendment filed on 6/30/2006.

2. The replacement sheets for the drawings have been entered.

3. Claims 1-3, 5-6, 8-16, 18-21, 23-28, 30, 32-34, 36, and 38 have been amended.

4. New claims 39-79 have been added and examined.

5. The objections and rejections from the prior correspondence not restated herein have been withdrawn.

### *Claim Objections*

6. Claims 53, 57, 72, and 76 are objected to under 37 CFR 1.75(c), as being of improper dependent form for failing the infringement test. Applicant is required to cancel the claim(s), or amend the claim(s) to place the claim(s) in proper dependent form, or rewrite the claim(s) in independent form.

See also MPEP 608.01 (n), "Infringement Test" for dependent claims. The test for a proper dependent claim is whether the dependent claim includes every limitation of the parent claim. The test is not whether the claims differ in scope. A proper dependent claim shall not conceivably be infringed by anything, which would not also infringe the basic claim.

The claims in question recite that the first edge is a falling edge, which directly contradicts their parent claim, which states that the first edge is a rising edge. Accordingly, the claims have not been examined with regard to prior art.

7. Claim 78 is objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim. Applicant is required to cancel the claim(s), or amend the claim(s) to place the claim(s) in proper dependent form, or rewrite the claim(s) in independent form.

### *Claim Rejections - 35 USC § 112*

8. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

9. Claims 21-27, 45-46, 53, 57, 72, 76 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

10. Claim 21 and 24 recites the limitation "the multiple command and address pins" in lines 7 and 12 of each claim. There is insufficient antecedent basis for this limitation in each claim.

11. Claims 53, 57, 72, 76, recite the limitation, "the first edge is a falling edge," which directly contradicts the parent claims which state the first edge is a rising edge. This renders the claims indefinite and obscures the metes and bounds that the applicant intends to claim.

### *Claim Rejections - 35 USC § 102*

12. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

13. Claims 15-17, 21-23, 28-38, 43, 45, 47-48, rejected under 35 U.S.C. 102(b) as being anticipated by DeMone et al., US patent 6266750.

14. With respect to claim 15, DeMone teaches of a memory device comprising: multiple command and address pins to receive a first portion of an F-bit word, wherein F is a positive integer, wherein the F-bit word comprises a set of command and address signals, wherein the first portion of the F-bit word comprises a first subset of the set of command and address signals, wherein multiple command and address pins receive the first portion of the F-bit word substantially simultaneous with receiving a first edge of a clock signal, wherein the multiple command and address pins to further receive a second portion of an F-bit word, wherein the second portion of the F-bit word comprises a second subset of the set of command and address signals, wherein the multiple command and address pins receive the second portion of the F-bit word substantially simultaneous with receiving a second edge of a clock signal (fig. 1, 3a-b; column 3, lines 20-30; column 3, lines 44-51; column 3, line 61-column 4, line 5; column 4, lines 29-33; as the SLDRAM is an IC (integrated circuit), there must be I/O pins connecting to the command link to enable the signals to be received from the command module as described. As there are 10 command/address lines, there must be 10 pins, which allow for the signals to be transferred from the memory chip; without the pins, the memory would not be connected to the CA[0:9] bus), and

wherein the memory device operates to perform a memory command in response to the set of received command and address signals (fig. 5a, column 5, lines 10-32).

15. With respect to claim 21, DeMone teaches of the limitations cited above with respect to claim 15. DeMone also teaches of memory circuit comprising: one or more integrated circuit memory devices operable for communicating with an external controller (fig. 1; column 3, lines 20-30; where the SLDRAMs are individual ICs (integrated circuits) connected to a command module).

16. With respect to claim 28, DeMone teaches of a system comprising: one or more integrated circuit memory devices, wherein each of the one or more integrated circuit memory devices includes multiple data, command, and address pins (fig. 1; column 3, lines 20-30; column 4, lines 28-35; where the SLDRAMs are individual ICs (integrated circuits). As the ICs must be able to connect to the command link and data links, they each must have pins that provide electrical connectivity from the desired location, through the ICs' housing to the circuitry. Since there are 10 individual command/address lines (10 bits) there must be 10 pins); and

a bus, wherein the one or more integrated circuit memory devices are coupled via the bus to a controller through the multiple data, command, and address pins (fig. 1, 2a; column 3, lines 20-35, column 4, lines 28-35; where the data links connect the memory devices to the command module. They must be connected through the pins in the IC),

wherein the controller operates to send a word comprising command and address signals during a clock cycle of a clock signal such that the number of bits in the word sent from the controller to the integrated circuit memory device is higher than a given number of command and address pins in each integrated circuit memory device (fig. 3a-b; column 3, lines 20-30, lines 44-51; column 3, line 61-column 4, line 5; column 4, lines 28-35; there are 4 consecutive 10-bit packets that are received and then combined into a 40-bit packet (a word). Each bit of 4 packets cannot be transmitted at the same time as there are only 10 bits worth of lines and pins).

17. With respect to claim 32, DeMone teaches of a semiconductor circuit comprising: one or more integrated circuit memory devices, wherein each integrated circuit memory device comprises multiple command and address pins, wherein the command and address pins of each integrated circuit memory device are coupled to receive words comprising command and address signals (fig. 1; column 3, lines 20-30; column 4, lines 28-35; where the SLDRAMs are individual ICs (integrated circuits). As the ICs must be able to connect to the command link and data links, they each must have pins that provide electrical connectivity from the desired location, through the ICs' housing to the circuitry. Since there are 10 individual command/address lines (10 bits) there must be 10 pins; the 40-bit packet received over four 10-bit transmissions makes up a word),

wherein the memory devices operate to receive words during a clock cycle of a clock signal such that the number of bits in the words sent to each integrated circuit memory device is higher than the multiple command and address pins available in each integrated circuit memory device (fig. 3a-b; column 3, lines 20-30, lines 44-51; column

3, line 61-column 4, line 5; column 4, lines 28-35; there are four consecutive 10-bit packets that are received and then combined into a 40-bit packet (word). The signals of four packets cannot be transmitted at the same time as there are only 10 bits worth of lines and pins).

18. With respect to claim 36, DeMone teaches of a memory circuit comprising: one or more integrated circuit memory devices, wherein each integrated circuit memory device comprises a predetermined number of command and address pins (fig. 1; column 3, lines 20-30; column 4, lines 28-35; where the SLDRAMs are individual ICs (integrated circuits). As the ICs must be able to connect to the command link and data links, they each must have pins that provide electrical connectivity from the desired location, through the ICs' housing to the circuitry. Since there are 10 individual command/address lines (10 bits) there must be 10 pins. Since the number of pins is decide before fabrication of the IC, the quantity of 10 corresponding to each command/address line must have been predetermined),

wherein each integrated circuit memory device is coupled to send and receive signals on the predetermined number of command and address pins, wherein the one or more memory devices operates to receive a word comprising a number of command and address signals during more than one edge of a clock signal such that the number of bits in each word for each integrated circuit memory device are substantially higher than the predetermined number of command and address pins in each integrated circuit memory device (fig. 3a-b; column 3, lines 20-30, lines 44-51; column 3, line 61-column 4, line 5; column 4, lines 28-35; there are four consecutive 10-bit packets that are

received and then combined into a 40-bit packet (word). The signals of the four packets cannot be transmitted at the same time as there are only 10 bits worth of lines and pins).

19. With respect to claims 16, 23, 30, 33, DeMone teaches of wherein the memory device comprises a device selected from the group consisting of a DRAM device, a flash memory device, a non-volatile memory device, a static random access memory (SRAM) device, and a static memory device (fig. 1-2; column 3, lines 20-42;. the memory device is a SLDRAM which is a type of DRAM).

20. With respect to claims 17, and 22, DeMone teaches of wherein the first and second edges of the clock signal comprise rising and falling edges of the clock signal, respectively, wherein in the rising and falling edges comprise a transition from a logic level "zero" to a logic level "one" and a transition from the logic level "one" to the logic level "zero", respectively (fig. 3b; column 3, lines 44-51; column 3, line 61-column 4, line 5).

21. With respect to claim 29, DeMone teaches of in sending, the external controller is a device selected from the group consisting of a DRAM controller, a central processing unit (CPU), a graphics processing unit (GPU), and a processor (fig. 1; column 3, lines 22-30; as the command module, implemented by a memory controller, controls a type of DRAM, it must be a DRAM controller).

22. With respect to claim 31, DeMone teaches of wherein the controller is operable for sending the command and address signals during the clock cycle of the clock signal comprises sending the command and address signals upon both rising and falling

edges of the clock cycle when transferring data to and from each integrated circuit memory device (fig. 3b; column 3, lines 44-51; column 3, line 61-column 4, line 5).

23. With respect to claims 34 and 38, DeMone teaches of wherein the command and address signals during the clock cycle of the clock signal are initiated from the group consisting of initiating the command and address signals upon both the rising and falling edges of the clock cycle of the clock signal, initiating the command and address signals upon a rising edge of the clock cycle and further initiating address signals on a falling edge of the clock cycle, initiating the command and address signals upon two consecutive rising edges of the clock signal, and initiating the command and address signals on a rising edge of the clock cycle and further initiating the address signals on a subsequent rising edge of the clock cycle (fig. 3b; column 3, lines 44-51; column 3, line 61-column 4, line 5).

24. With respect to claim 37, DeMone teaches of wherein the integrated circuit memory device is a DRAM device (fig. 1; column 3, lines 20-30; where the IC is a SLDRAM a type of DRAM).

25. With respect to claims 43, 45, 47, 48, DeMone teaches of wherein the integrated circuit memory device is a volatile memory device (fig. 1; column 3, lines 20-30; where the IC is a SLDRAM a type of DRAM, which is a type of volatile memory).

### *Claim Rejections - 35 USC § 103*

26. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

27. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

28. Claims 1-4, 39, 49-52, 54, 58-59, 61-71, 73, 78-79 rejected under 35 U.S.C. 103(a) as being unpatentable over DeMone et al., US patent 6266750, and Schaefer, US patent 5666321.

29. With respect to claim 1, DeMone teaches of a method of operating a memory device, comprising: receiving an F-bit word, wherein F is a positive integer, wherein the F-bit word comprises a set of command and address signals (column 3, lines 44-51; column 4, lines 29-33; the 40-bit command packet is a word),

wherein receiving the F-bit word comprises: receiving a first portion of the F-bit word substantially simultaneous with receiving a first edge of a clock signal (fig. 3a-b; column 3, lines 44-51; column 3, line 61-column 4, line 5; column 4, lines 29-33; where F is 40 bits),

wherein the first portion of the F-bit word comprises G-bits, wherein G is less than F, wherein the G-bit portion comprises a first subset of a set of command and address signals (column 4, lines 29-33; where the 10-bits parts are combined to form a

40-bit command packet (word). G is 10 bits, which is less than 40. It is abundantly clear to one of ordinary skill in the art that the command packet can be considered a word since the packet in its entirety is needed to access the memory); and

receiving a second portion of the F-bit word substantially simultaneous with receiving a second edge of the clock signal (fig. 3a-b; column 3, lines 44-51; column 3, line 61-column 4, line 5),

wherein the second portion of the F-bit word comprises H-bits, wherein the H-bit portion comprises a second subset of the set of command and address signals (column 4, lines 29-33; where the 10-bits parts are combined to form a 40-bit command packet (word). H is 10 bits),

performing a memory command in response to the received F-bit word (fig. 5a, column 5, lines 10-32).

Schaefer teaches of wherein H is F-G (column 1, lines 28-32; where the memory address is broken down into two parts. Thus the size of the second part is equal to the size of the entire address minus the size of the first part).

It would have been obvious to one of ordinary skill in the art having the teachings of DeMone and Schaefer at the time of the invention to use two (or any other number) 10-bit groups to make the command packet of DeMone as taught in Schaefer. Their motivation would have been to enable the invention of DeMone to operate with different memories which require different sized command words/packets.

30. With respect to claim 2, DeMone teaches of wherein the memory device comprises a device selected from the group consisting of a DRAM device, a flash

memory device, a non-volatile memory device, a static random access memory (SRAM) device, and a static memory device (fig. 1-2; column 3, lines 20-42; the memory device is a SLDRAM which is a type of DRAM).

31. With respect to claim 3, DeMone teaches of sending the first portion of the F-bit word substantially simultaneous with sending the first edge of the clock signal by an external controller; and sending the second portion of the F-bit word substantially simultaneous with sending the second edge of the clock signal by the external controller (fig. 1, 2a, 3b; column 3, lines 22-30; column 3, line 61-column 4, line 5; where the command module sends the command/address signals and the clock signal).

32. With respect to claim 4, DeMone teaches of in sending, the external controller is a device selected from the group consisting of a DRAM controller, a central processing unit (CPU), a graphics processing unit (GPU), and a processor (fig. 1; column 3, lines 22-30; as the command module, implemented by a memory controller, controls a type of DRAM, it must be a DRAM controller).

33. With respect to claim 39, DeMone teaches of wherein the integrated circuit memory device is a volatile memory device (fig. 1; column 3, lines 20-30; where the IC is a SLDRAM a type of DRAM, which is a type of volatile memory).

34. With respect to claim 49, DeMone teaches of receiving an F-bit word using J command and address pins of a programmable memory device, wherein F and J are positive integers, wherein J is less than F, wherein the F-bit word comprises a set of command and address signals (fig. 1; column 3, lines 44-51; column 4, lines 29-33; the

40-bit command packet is a word, F is 40 and J is 10 as the CA[0:9] bus has a 10-bit capacity and must have 10 pins going into the SLDRAM module), comprising:

receiving a first portion of the F-bit word at a first time, wherein the first portion of the F-bit word comprises G-bits, wherein G is less than F, wherein G is less than or equal to J (fig. 3b; column 4, lines 29-33; where the 10-bits parts are combined to form a 40-bit command packet (word). G is 10 bits, which is less than 40 bits, which is also equal to the 10 pins into the module);

receiving a second portion of the F-bit word at a second time, wherein the second portion of the F-bit word comprises H-bits, wherein H is less than or equal to J (fig. 3a-b; column 3, lines 44-51; column 3, line 61-column 4, line 5; column 4, lines 29-33; where the 10-bits parts are combined to form a 40-bit command packet (word). H is 10 bits, which is less than 40 and equal to the 10 pins); and

performing a memory command in response to the fully-received F-bit word (fig. 5a, column 5, lines 10-32).

Schaefer teaches of wherein H is F-G (column 1, lines 28-32; where the memory address is broken down into two parts. Thus the size of the second part is equal to the size of the entire address minus the size of the first part).

It would have been obvious to one of ordinary skill in the art having the teachings of DeMone and Schaefer at the time of the invention to use two (or any other number) 10-bit groups to make the command packet of DeMone as taught in Schaefer. Their motivation would have been to enable the invention of DeMone to operate with different memories which require different sized command words/packets.

35. With respect to claims 50-52, DeMone teaches of wherein a first time includes at or substantially simultaneously with receiving a first rising edge of a first clock cycle of a clock signal (fig. 3b; where A0 is received on the rising edge of a first period of the clock (CCLK)).

36. With respect to claim 54, DeMone teaches of wherein a second time includes at or substantially simultaneously with receiving a second edge of a clock signal (fig. 3b; where A1 is received on a second edge of the clock signal (CCLK)).

37. With respect to claims 58-59, DeMone teaches of wherein the G-bit portion of the F-bit word comprises a first subset of a set of command and address signals (column 3, lines 44-51; column 4, lines 29-34).

38. With respect to claims 61-64, DeMone teaches of wherein the H-bit portion comprises a second subset of command and address signals (column 3, lines 44-51; column 4, lines 29-34; where the second 10-bit portion also includes command/address signals, thus it also includes address signals. As they are in the second portion, they are the second subset of such signals).

39. With respect to claim 65, DeMone teaches of wherein a programmable memory device includes a device selected from the group consisting of a DRAM device, a SRAM device, a static memory device, a flash memory device, and a non-volatile memory device (fig. 1; column 3, lines 20-30; where the IC is a SLDRAM a type of DRAM).

40. With respect to claim 66, DeMone teaches of wherein a programmable memory device includes a volatile memory device (fig. 1; column 3, lines 20-30; where the IC is a SLDRAM a type of DRAM, which is a type of volatile memory).

41. With respect to claim 67, DeMone teaches of sending the first portion of the F-bit word with a controller at a first time; and sending the second portion of the F-bit word with a controller at a second time (fig. 1, 2a, 3b; column 3, lines 22-30; column 3, line 61-column 4, line 5; where the command module sends the command/address signals and the clock signal).

42. With respect to claim 68, DeMone teaches of wherein a controller is a device selected from the group consisting of a DRAM controller, a central processing unit (CPU), a graphics processing unit (GPU), and a processor (fig. 1; column 3, lines 22-30; as the command module, implemented by a memory controller, controls a type of DRAM, it must be a DRAM controller).

43. With respect to claims 69-71 and 73, DeMone teaches of the limitations as cited above with respect to claims 50-52 and 54, respectively.

44. With respect to claim 78, DeMone teaches of the limitations cited with respect to claim 49 above.

45. With respect to claim 79, Schaefer teaches of wherein address signals consist of row address data (column 1, lines 28-35).

46. Claims 5-14, 40-42, 55-56, 60, 74-75, 77 are rejected under 35 U.S.C. 103(a) as being unpatentable over DeMone, Schaefer, and Ohshima et al., US patent application publication 2001/0006483.

47. With respect to claim 5, DeMone teaches of a method of operating a memory device, comprising: receiving an F-bit word, wherein F is a positive integer, wherein the

F-bit word comprises a set of command and address signals (column 3, lines 44-51; column 4, lines 29-33),

wherein receiving the F-bit word comprises: receiving a first portion of the F-bit word substantially simultaneous with receiving a first edge of a clock signal (fig. 3a-b; column 3, lines 44-51; column 3, line 61-column 4, line 5; packet A0);

wherein the first portion of the F-bit word comprises G-bits, wherein G is less than F (column 4, lines 29-33; where the 10-bits parts are combined to form a 40-bit command packet (word). G is 10 bits, which is less than 40. It is abundantly clear to one of ordinary skill in the art that the command packet can be considered a word since the packet in its entirety is needed to access the memory);

receiving a second portion of the F-bit word (fig. 3a-b; column 3, lines 44-51; column 3, line 61-column 4, line 5; packet A2),

wherein the second portion of the F-bit word comprises H-bits (column 4, lines 29-33; where the 10-bits parts are combined to form a 40-bit command packet (word). H is 10 bits, which is less than 40); and

performing a memory command in response to the received F-bit word (fig. 5a, column 5, lines 10-32).

Ohshima teaches of wherein the G-bit portion comprises a set of command signals and a first subset of a set of address signals (fig. 17; paragraph 0084; where the read command (command signals) and the upper address (1$^{st}$ part of the address) is received on the rising edge of the 1$^{st}$ clock cycle),

wherein the H-bit portion comprises a second subset of the set of address signals (fig. 17; paragraph 0084; where the lower address (2nd part of the address) is received on the rising edge of the 2nd clock cycle),

Schaefer teaches of wherein H is F-G (column 1, lines 28-32; where the memory address is broken down into two parts. Thus the size of the second part is equal to the size of the entire address minus the size of the first part).

It would have been obvious to one of ordinary skill in the art having the teachings of DeMone, and Ohshima at the time of the invention to include the command signals and part of the address with the first portion and output the address with the second portion in DeMone as taught in Ohshima. Their motivation would have been to enhance the memory cell access speed without degrading the random access time (Ohshima, paragraph 0085).

It would have been obvious to one of ordinary skill in the art having the teachings of DeMone, Ohshima, and Schaefer at the time of the invention to use two (or any other number) 10-bit groups to make the command packet of the combination of DeMone and Ohshima as taught in Schaefer. Their motivation would have been to enable the combination of DeMone and Ohshima to operate with newer and older memories which require different sized command words/packets.

48. With respect to claim 8, DeMone teaches of a method of operating a memory device, comprising: receiving an F-bit word, wherein F is a positive integer, wherein the F-bit word comprises a set of command and address signals (column 3, lines 44-51; column 4, lines 29-33),

wherein receiving the F-bit word comprises: receiving a first portion of the F-bit word substantially simultaneous with receiving a first edge of a first cycle of a clock signal (fig. 3a-b; column 3, lines 44-51; column 3, line 61-column 4, line 5; packet A0);

wherein the first portion of the F-bit word comprises G-bits, wherein G is less than F, wherein the G-bit portion comprises a first subset of a set of command and address signals (column 4, lines 29-33; where the 10-bits parts are combined to form a 40-bit command packet (word). G is 10 bits, which is less than 40. It is abundantly clear to one of ordinary skill in the art that the command packet can be considered a word since the packet in its entirety is needed to access the memory);

receiving a second portion of the F-bit word (fig. 3a-b; column 3, lines 44-51; column 3, line 61-column 4, line 5; packet A2),

wherein the second portion of the F-bit word comprises H-bits, wherein the H-bit portion comprises a second subset of the set of command and address signals (column 4, lines 29-33; where the 10-bits parts are combined to form a 40-bit command packet (word). H is 10 bits, which is less than 40); and

performing a memory command in response to the received F-bit word (fig. 5a, column 5, lines 10-32).

Ohshima teaches of wherein the second portion of the F-bit word is received substantially simultaneous with receiving a first edge of a second cycle of a clock signal (fig. 17; paragraph 0084).

Schaefer teaches of wherein H is F-G (column 1, lines 28-32; where the memory address is broken down into two parts. Thus the size of the second part is equal to the size of the entire address minus the size of the first part).

It would have been obvious to one of ordinary skill in the art having the teachings of DeMone, and Ohshima at the time of the invention to output the second portion based on the rising edge of the next clock cycle in DeMone as taught in Ohshima. Their motivation would have been to allow a wider range of memory types to be used, with the same supporting circuitry lowering the cost.

It would have been obvious to one of ordinary skill in the art having the teachings of DeMone, Ohshima, and Schaefer at the time of the invention to use two (or any other number) 10-bit groups to make the command packet of the combination of DeMone and Ohshima as taught in Schaefer. Their motivation would have been to enable the combination of DeMone and Ohshima to operate with newer and older memories which require different sized command words/packets.

49. With respect to claim 11, DeMone teaches of a method of operating a memory device, comprising: receiving an F-bit word, wherein F is a positive integer, wherein the F-bit word comprises a set of command and address signals (column 3, lines 44-51; column 4, lines 29-33),

wherein receiving the F-bit word comprises: receiving a first portion of the F-bit word substantially simultaneous with receiving a first edge of a first cycle of a clock signal (fig. 3a-b; column 3, lines 44-51; column 3, line 61-column 4, line 5; packet A0);

wherein the first portion of the F-bit word comprises G-bits, wherein G is less than F (column 4, lines 29-33; where the 10-bits parts are combined to form a 40-bit command packet (word). G is 10 bits, which is less than 40. It is abundantly clear to one of ordinary skill in the art that the command packet can be considered a word since the packet in its entirety is needed to access the memory);

receiving a second portion of the F-bit word (fig. 3a-b; column 3, lines 44-51; column 3, line 61-column 4, line 5; packet A2),

wherein the second portion of the F-bit word comprises H-bits (column 4, lines 29-33; where the 10-bits parts are combined to form a 40-bit command packet (word). H is 10 bits, which is less than 40); and

performing a memory command in response to the received F-bit word (fig. 5a, column 5, lines 10-32).

Ohshima teaches of wherein the G-bit portion comprises a set of command signals and a first subset of a set of address signals (fig. 17; paragraph 0084; where the read command (command signals) and the upper address (1st part of the address) is received on the rising edge of the 1st clock cycle),

wherein the H-bit portion comprises a second subset of the set of address signals (fig. 17; paragraph 0084; where the lower address (2nd part of the address) is received on the rising edge of the 2nd clock cycle),

wherein the second portion of the F-bit word is received substantially simultaneous with receiving a first edge of a second cycle of a clock signal (fig. 17;

paragraph 0084; where the lower address (2nd part of the address) is received on the rising edge of the 2nd clock cycle).

Schaefer teaches of wherein H is F-G (column 1, lines 28-32; where the memory address is broken down into two parts. Thus the size of the second part is equal to the size of the entire address minus the size of the first part).

It would have been obvious to one of ordinary skill in the art having the teachings of DeMone, and Ohshima at the time of the invention to include the command signals and part of the address with the first portion and output the address with the second portion in DeMone as taught in Ohshima. Their motivation would have been to enhance the memory cell access speed without degrading the random access time (Ohshima, paragraph 0085).

It would have been obvious to one of ordinary skill in the art having the teachings of DeMone, and Ohshima at the time of the invention to output the second portion based on the rising edge of the next clock cycle in DeMone as taught in Ohshima. Their motivation would have been to allow a wider range of memory types to be used, with the same supporting circuitry lowering the cost.

It would have been obvious to one of ordinary skill in the art having the teachings of DeMone, Ohshima, and Schaefer at the time of the invention to use two (or any other number) 10-bit groups to make the command packet of the combination of DeMone and Ohshima as taught in Schaefer. Their motivation would have been to enable the combination of DeMone and Ohshima to operate with newer and older memories which require different sized command words/packets.

50. With respect to claims 9 and 12, DeMone teaches of wherein, in receiving the second portion of the F-bit word, the second cycle is substantially subsequent to the first cycle (fig. 3b; column 3, line 61-column 4, line 5).

51. With respect to claims 6, 10, and 14, DeMone teaches of wherein the memory device comprises a device selected from the group consisting of a DRAM device, a flash memory device, a non-volatile memory device, a static random access memory (SRAM) device, and a static memory device (fig. 1-2; column 3, lines 20-42; the memory device is a SLDRAM which is a type of DRAM).

52. With respect to claim 7, DeMone teaches of wherein the first and second edges of the clock signal comprise rising and falling edges of the clock signal, respectively, wherein in the rising and falling edges comprise a transition from a logic level "zero" to a logic level "one" and a transition from the logic level "one" to the logic level "zero", respectively (fig. 3b; column 3, lines 44-51; column 3, line 61-column 4, line 5).

53. With respect to claim 13, DeMone teaches of wherein a clock signal comprises a first and second edge, wherein the first and second edges of the clock signal comprise rising and falling edges of the clock signal, respectively, wherein in the rising and falling edges comprise a transition from a logic level "zero" to a logic level "one" and a transition from the logic level "one" to the logic level "zero", respectively (fig. 3b; column 3, lines 44-51; column 3, line 61-column 4, line 5).

54. With respect to claims 40-42, DeMone teaches of wherein the integrated circuit memory device is a volatile memory device (fig. 1; column 3, lines 20-30; where the IC is a SLDRAM a type of DRAM, which is a type of volatile memory).

55. With respect to claims 55-56 Ohshima teaches of wherein the second edge of a clock signal includes a first rising edge of a second cycle of the clock signal (fig. 17; where the lower address (LA) is received on the rising edge of the second clock period).

It would have been obvious to one of ordinary skill in the art having the teachings of DeMone, and Ohshima at the time of the invention to output the second portion based on the rising edge of the next clock cycle in DeMone as taught in Ohshima. Their motivation would have been to allow a wider range of memory types to be used, with the same supporting circuitry lowering the cost.

56. With respect to claim 60, Ohshima teaches of wherein the command and address signals comprise a set of command signals and a first subset of a set of address signals (fig. 17; paragraph 0084).

57. It would have been obvious to one of ordinary skill in the art having the teachings of DeMone, and Ohshima at the time of the invention to include the command signals and part of the address with the first portion and output the address with the second portion in DeMone as taught in Ohshima. Their motivation would have been to enhance the memory cell access speed without degrading the random access time (Ohshima, paragraph 0085).

58. With respect to claims 74-75, Ohshima teaches of the limitations as cited above with respect to claims 55-56.

59. With respect to claim 77, Ohshima teaches of wherein H and G are not equal to each other (fig. 17; paragraph 0084, as the G-bit section includes the command and the upper address, and the H-bit section includes just the lower address, it is abundantly

clear to one of ordinary skill in the art that H does not equal G, since it is clear that the upper and lower address portions are the same size).

60. Claims 18-20, 24-27, 44, and 46 are rejected under 35 U.S.C. 103(a) as being unpatentable over DeMone and Ohshima et al., US patent application publication 2001/0006483.

61. With respect to claim 18, the combination of DeMone and Ohshima teach of all the limitations of claim 18 cited above with respect to claim 8.

Additionally, DeMone inherently discloses multiple command and address pins to receive the first and second portions of the F-bit word (fig. 1; column 3, lines 20-30; as the SLDRAM is an IC (integrated circuit), there must be I/O pins connecting to the command link to enable the signals to be received from the command module as described. As there are 10 command/address lines, there must be 10 pins, which allow for the signals to be transferred from the memory chip; without the pins, the memory would not be connected to the CA[0:9] bus).

62. With respect to claim 24, DeMone teaches of all the limitations cited above with respect to claim 21. Ohshima teaches of wherein the second portion of the F-bit word is received substantially simultaneous with receiving a first edge of a second cycle of a clock signal (fig. 17; paragraph 0084).

It would have been obvious to one of ordinary skill in the art having the teachings of DeMone, and Ohshima at the time of the invention to output the second portion based on the rising edge of the next clock cycle in DeMone as taught in Ohshima. Their

motivation would have been to allow a wider range of memory types to be used, with the same supporting circuitry lowering the cost.

63. With respect to claims 19 and 27, DeMone teaches of wherein the memory device comprises a device selected from the group consisting of a DRAM device, a flash memory device, a non-volatile memory device, a static random access memory (SRAM) device, and a static memory device (fig. 1-2; column 3, lines 20-42; the memory device is a SLDRAM which is a type of DRAM).

64. With respect to claims 20, and 26, DeMone teaches of wherein a clock signal comprises a first and second edge, wherein the first and second edges of the clock signal comprise rising and falling edges of the clock signal, respectively, wherein in the rising and falling edges comprise a transition from a logic level "zero" to a logic level "one" and a transition from the logic level "one" to the logic level "zero", respectively (fig. 3b; column 3, lines 44-51; column 3, line 61-column 4, line 5).

65. With respect to claim 25, DeMone teaches of wherein, in receiving the second portion of the F-bit word, the second cycle is substantially subsequent to the first cycle (fig. 3b; column 3, line 61-column 4, line 5).

66. With respect to claims 44 and 46, DeMone teaches of wherein the integrated circuit memory device is a volatile memory device (fig. 1; column 3, lines 20-30; where the IC is a SLDRAM a type of DRAM, which is a type of volatile memory).

***Response to Arguments***

67. Applicant's arguments filed 6/30/2006 have been fully considered but they are not persuasive.

68. Applicant's arguments with respect to claims 8, 15, 18, 24, 32, 36 fail to comply with 37 CFR 1.111(b) because they amount to a general allegation that the claims define a patentable invention without specifically pointing out how the language of the claims patentably distinguishes them from the references. In order to do this, the applicant must discuss both the claim language ***and the cited references***.

69. With respect to claim 1, 28 the applicant argues that DeMone fails to teach of receiving an F-bit word in a first portion on a first clock edge and a second portion on a second clock edge. The examiner disagrees. Column 4, lines 29-33 of DeMone teaches of receiving four 10-bit words (portions) which are assembled into a 40-bit command packet (F-bit word) which is then decoded and used by the memory. These four 10-bit words include two portions, actually they are 4 portions, but if you have 4 you also have two, and the final command packet can be interpreted as a word since the 40-bit packet as a whole is needed and decoded for the memory to use, not each 10-bit word. Figure 3B shows that this occurs on consecutive clock edges on the CA{9:0] bus. The applicant further argues that the four 10-bit words are them selves separately complete. If they were complete, then they would not need to be assembled into a 40-bit word/packet before they can be used.

70. With respect to claim 21, the applicant argues that DeMone fails to teach of an F-bit word comprising a set of command and address signals broken into ***two*** portions. The examiner disagrees. Column 4, lines 29-33 of DeMone shows this being done with

four portions. As the claim language uses "comprising" the applied reference can show more than what is claimed, i.e. four portions. There are two groups of two portions within four portions.

71. Applicant's arguments with respect to claims 5-7 and 11-14 have been considered but are moot in view of the new ground(s) of rejection.

***Conclusion***

72. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

73. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

74. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

75. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael Krofcheck whose telephone number is 571-272-8193. The examiner can normally be reached on Monday - Friday.

76. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt Kim can be reached on 571-272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

77. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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